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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,961	07/15/2003	Shafqat Ahmed	42P13230D	7797

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EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,961	AHMED ET AL.	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *48-69* is/are pending in the application.

4a) Of the above claim(s) *50,57,58,66 and 67* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *48,49,51-56,59-65,68 and 69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/6/06 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 48 and 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter, U.S. Patent 4,356,623 in view of Shields et al., U.S. Patent 6,350,696.

Hunter shows the invention substantially as claimed including a method comprising: forming insulating spacers (7,8) adjacent to sidewalls of a gate by forming an insulating layer and removing a portion of the insulating layer that is not on the sidewalls; forming extension regions (for example, 10) after forming the insulating spacers by ion implantation using the insulating spacers as a mask; and forming a source and drain (for example, 13,14) by ion implantation, wherein the extension regions are shallower than the source and drain, and wherein the source and the drain are more heavily doped than the extension regions (see figs. 2-6 and col. 6-line 62 to col. 7-line 56).

Hunter does not expressly disclose forming insulating spacers by a combination of a dry etch and then a wet etch.

Shields et al. discloses forming a spacer by a combination of a dry etch and then a wet etch (see figs. 4-7 and col. 3-lines 10-65). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Hunter so as to form the spacers using a dry and wet etch combination as disclosed by Shields et al. because such a process will prevent the damage of the silicon and gate insulating layer from the plasma etching process.

Concerning the thickness of the spacer, Shields et al. discloses leaving about 200-400 angstroms of spacer material (see col. 3-line 44) which constitutes an overlapping range thereby establishing a prima facie case of obviousness with the 10-

200 angstrom range. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum spacer thickness depending upon, for example, the desired degree of protection from leakage or overlap capacitance and would not lend patentability to the instant application absent the showing of unexpected results.

Claims 53-54 and 59-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter, U.S. Patent 4,356,623 in view of Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology".

Hunter is applied as above but does not expressly disclose the spacers being formed by LPCVD at a temperature higher than seven hundred fifty Celsius.

Wolf et al. discloses forming silicon dioxide using LPCVD in a temperature range overlapping the claimed range (see last two paragraphs on page 184). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Hunter so as to form the spacers using the process disclosed by Wolf et al. because such films show excellent conformability.

Concerning the thickness of the spacer, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum spacer thickness depending upon, for example, the desired degree of protection from leakage or overlap capacitance and would not lend patentability to the instant application absent the showing of unexpected results.

Claim 56 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter, U.S. Patent 4,356,623 in view of Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology" as applied to claims 53-54 and 59-60 above, and further in view of Shields et al., U.S. Patent 6,350,696.

Hunter and Wolf et al. do not expressly disclose forming insulating spacers by a combination of a dry etch and then a wet etch.

Shields et al. discloses forming a spacer by a combination of a dry etch and then a wet etch (see figs. 4-7 and col. 3-lines 10-65). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Hunter modified by Wolf et al. so as to form the spacers using a dry and wet etch combination as disclosed by Shields et al. because such a process will prevent the damage of the silicon and gate insulating layer from the plasma etching process.

Claims 48-49, 51-52, 61-63, and 68-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bracco et al., U.S. Patent 4,536,944 in view of Shields et al., U.S. Patent 6,350,696.

Bracco et al. shows the invention substantially as claimed including a method comprising: forming insulating spacers (14,18) adjacent to sidewalls of a gate by forming an insulating layer and removing a portion of the insulating layer that is not on the sidewalls; forming extension regions (22,24) after forming the insulating spacers by ion implantation using the insulating spacers as a mask; and forming a source and drain

(see fig. 5) by ion implantation, wherein the extension regions are shallower than the source and drain, wherein the source and the drain are more heavily doped than the extension regions, wherein the method further comprises removing the insulating spacers by performing a wet etch; and after said removing the insulating spacers, performing said forming the source and drain (see figs. 1-5 and col. 5-line 20 to col. 6-line 57).

Bracco et al. does not expressly disclose forming insulating spacers by a combination of a dry etch and then a wet etch.

Shields et al. discloses forming a spacer by a combination of a dry etch and then a wet etch (see figs. 4-7 and col. 3-lines 10-65). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Bracco et al. so as to form the spacers using a dry and wet etch combination as disclosed by Shields et al. because such a process will prevent the damage of the silicon and gate insulating layer from the plasma etching process.

Concerning the thickness of the spacer, Shields et al. discloses leaving about 200-400 angstroms of spacer material (see col. 3-line 44) which constitutes an overlapping range thereby establishing a prima facie case of obviousness with the 10-200 angstrom range. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum spacer thickness depending upon, for example, the desired degree of protection from leakage or overlap capacitance and would not lend patentability to the instant application absent the showing of unexpected results.

Claims 53-54 and 59-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bracco et al., U.S. Patent 4,536,944 in view of Shields et al., U.S. Patent 6,350,696 as applied to claims 48-49, 51-52, 61-63, and 68-69 above, and further in view of Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology".

Bracco et al. and Shields et al. are applied as above but do not expressly disclose the spacers being formed by LPCVD at a temperature higher than seven hundred fifty Celsius.

Wolf et al. discloses forming silicon dioxide using LPCVD in a temperature range overlapping the claimed range (see last two paragraphs on page 184). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Hunter so as to form the spacers using the process disclosed by Wolf et al. because such films show excellent conformability.

Concerning the thickness of the spacer, Shields et al. discloses leaving about 200-400 angstroms of spacer material (see col. 3-line 44) which constitutes an overlapping range thereby establishing a prima facie case of obviousness with the 10-200 angstrom range. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum spacer thickness depending upon, for example, the desired degree of protection from leakage or overlap capacitance and would not lend patentability to the instant application absent the showing of unexpected results.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard A. Booth
Primary Examiner
Art Unit 2812

March 9, 2006